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Selection of Inductor and Snubber Capactor to Optimize the Size and Efficiency of DC-DC Switching Power Converter

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***Abstract* - This paper presents a selection of inductor and snubber capacitor in non-isolated synchronous DC-DC switching power converter. The circuit is made to operate in Synchronous Discontinuous Conduction Mode (SDCM)/Forced Continuous Conduction Mode (FCCM) of operation for minimum inductor value, to reduce the size, weight and cost of the converter. The turn off loss of the switch induced by SDCM of operation is minimized by connecting snubber capacitor across the transistor switch. Before the switch is turned ON, snubber capacitor requires certain amount of energy must be stored in the inductor to discharge the capacitor energy [1]. The question is how much capacitor and inductor value is required. A series of MATLAB script are executed to find minimum inductor value for FCCM of operation and to select snubber capacitor for maximum efficiency. Complementary gate signals are used to control the ON and OFF of main and auxiliary switch. SDCM of operation due to complementary control gate signal scheme, minimum turn on loss of the transistor switch and low diode reverse recovery loss are achieved. Thus the Zero Voltage Resonant Transition (ZVRT) of transistor switch is realized, both turn on and turn off loss is minimized and also removes the parasitic ringing in inductor current.**
***Keywords*: SDCM, buck, boost, buck-boost, non-isolated, MATLAB script**

I. INTRODUCTION

Switching DC-DC converters are power electronic circuits which transfer one level of electrical voltage into another level by switching action. These converters are implemented in numerous fields like Uninterrupted Power Supplies (UPS), telecommunication purpose, DC machine drives, aerodynamics, hybrid electric and fuel cell vehicles[2][3], renewable energy system etc.The function of a DC-DC converter is to provide a stable DC output voltage from a given input voltage. The converter is typically required to regulate the DC output voltage given a range of load currents drawn and/or range of input voltage applied. Ideally the DC output is to be clean, that is with ripple current or voltage held below a specified level. Furthermore, the load power is to be delivered from the source with some specified level of efficiency. Power inductor selection is an important step to achieving these goals. Inductance is calculated to provide a cer tain minimum amount of energy storage and to reduce output current ripple. Using less than the calculated inductance causes increased AC ripple on the DC output. Using much greater or much less inductance may force the converter to change between continuous and discontinuous modes of operation.A smaller inductor value enables a faster transient response; it a lso results in larger current ripple, which causes higher conduction losses in the switches, inductor, and parasitic resistances. The smaller inductor also requires a larger filter capacitor to decrease the output voltage ripple [4]. The parasitic ringing effect due to turn-off loss (due to high switch current) can be minimizing by connecting snubber capacitor across the switch. A snubber is an energy-absorbing circuit used to eliminate voltage spikes caused by circuit parasitic inductance when a switch opens. Design process of snubber circuit for DC-DC converter and six topologies of snubber circuits (C, single C, RC, single RC, RCD, single RCD) were investigated in simulation tests [5]. This paper proposes an inductor and snubber capacitor optimization. A serial of MATLAB script are executed to find the optimum value of snubber capacitor and inductor based on the minimal overall device and switch conduction loss condition for maximum efficiency.

II. CIRCUIT TOPOLOGY

A non-isolated synchronous bidirectional switching DC-DC power converter technology is to combine a buck, boost and buck-boost mode of operation.Complementary gate signal control scheme is used to control the ON and OFF of transistor switches. The converter is operated in SDCM of operation such that the inductor size, cost, converter size and weight can be reduced. The SDCM of operation introduces more turn-off loss due to the main switch turn off during twice or higher load current [6]. This is one of the drawback of the inductor size reduction. The inductor current parasitic ringing will be caused by the oscillation of inductor with device output capacitance during turn off period of switch[7]. This issue due to SDCM of operation will affect the efficiency. The snubber capacitor added across the transistor switch is to reduce turn off loss. For zero turn-on loss the energy stored in the capacitor need to be discharged before the switch is turned ON, thus the Snubber capacitor requires certain amount of energy must be stored in the inductor to discharge the capacitor energy before the device is turned on. Thus the Zero Voltage Resonant Transition (ZVRT) of transistor switch is realized. The main advantage of the SDCM of operation due to complementary gating signal control scheme, is minimum

turn-on loss, thus low diode reverse recovery loss is achieved and also removes the parasitic ringing in inductor current. Thus both turn-on and -off losses are minimized. PID controller is used as a feedback controller in buck, boost and buck-boost mode of operation with inductor current as a feedback reference [8].

Fig.1 shows the circuit topology.When V_H= DC source voltage and V_L = 0 voltage, the circuit will act as buck mode with R_2 act as load and R_1 is the internal resistance of V_H. When V_H=0 V and V_L=DC source voltage, the circuit is in boost mode with R_1 as a load and R_2 is the internal resistance of V_L. In buck mode the inductor average current is positive and in boost mode it is negative. In buck-boost mode of operation,V_H and V_L are the source voltage at high side (V_1) and at low side (V_2) voltage respectively, R_1 is the internal resistance of V_H, R_2 is the load resistance at low voltage side.C_H and C_L are the input and output capacitors to smooth the load current and load voltage. Q_1 and Q_2 are MOSFETs, acts as switches with body diode D_1 and D_2 respectively. C_1 and C_2 are snubber capacitors. L is the inductor with effective series resistance R_{LP}.

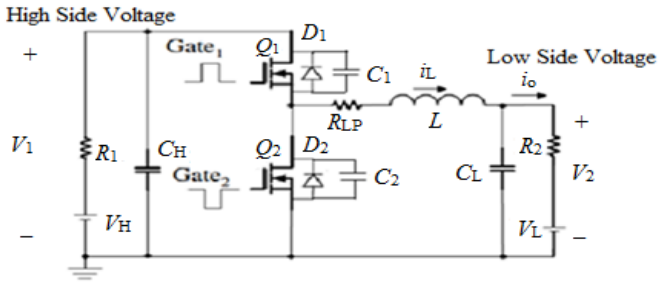

Fig. 1 Circuit topology

III. INDUCTOR SELECTION

The gate signal realization of complementary control over soft switching of ZVRT depends upon negative inductor current emergence, that will take place by limiting the inductance less than critical inductor (L_{cr}) value, given in equation (1) [9]. This inductance allows the converter operating under the boundary condition between FCCM and Continuous Conduction Mode (CCM) of operation.

$$L_{cr} = \frac{1}{2}.\frac{V_{in}-V_{out}}{P_o}.\frac{{V_{out}}^2}{V_{in}}.T_s \quad (1)$$

Where V_{in} is the input voltage, V_{out} is the output voltage, P_o is output power and T_s is the switching frequency.

The inductor ripple current (ΔI_L) [10] and the inductor conduction loss (P_L) [11] are given in equation (2) and (3) respectively.

$$\Delta I_L = \frac{1}{2}.\frac{V_{in}-V_{out}}{L}.\frac{V_{out}}{V_{in}}.T_s \quad (2)$$

$$P_L = I^2_{RMS_L}.R_{LP} \quad (3)$$

Where R_{LP} is the effective series resistance (ESR) of the inductor L and I_{RMS_L} is the rms inductor current given in equation (4)

$$I^2_{RMS\_L} = I^2_L + \frac{{\Delta I_L}^2}{12} \quad (4)$$

Where I_L is the inductor average current.

TABLE I INDUCTOR SELECTION

Mode of operation	Case	V_H (V)	V_L (V)	R_1 (Ω)	R_2 (Ω)	I* (A)	L_{cr} (µH)	Boundary Condition		FCCM of operation	
								ΔI_{Lcr} (A)	P_{Lcr} (W)	$\Delta I_{L\text{-}10\mu H}$ (A)	$P_{L\text{-}10\mu H}$ (W)
Buck	1	250	0	10m	10	15	39.97	15	8.77	59.96	18.88
	2	250	0	10m	10	20	19.94	20	15.60	39.89	19.17
	3	250	0	10m	5	20	29.99	20	15.60	59.98	25.19
	4	270	0	10m	10	15	44.42	15	8.77	66.64	21.42
Boost	1	0	50	18	10m	-12	21.79	11.79	5.60	25.70	7.16
	2	0	60	18	10m	-12	23.77	11.82	5.60	28.12	7.55
	3	0	60	18	10m	-16	20.57	15.69	9.95	32.30	12.34
	4	0	60	9	10m	-12	12.65	11.82	5.60	14.97	5.85
Buck-Boost	1	250	110	10m	2	30	18.10	30	35.10	54.30	41.24
		250	110	10m	2	-20	25.20	20	15.60	50.40	22.02
	2	250	110	10m	1	30	20.51	30	35.10	61.54	43.76
		250	110	10m	1	-20	28.80	20	15.60	57.60	24.35
	3	260	110	10m	2	30	19.58	30	35.10	58.76	42.75
		260	110	10m	2	-20	25.57	20	15.60	51.15	22.25

A series of MATLAB script are executed, to find minimum inductor value for FCCM of operation. The results are tabulated in Table 1. The switching time considered is 0.02 ms. From the Table 1, it is observed that, the minimum and maximum inductor value at boundary condition is 12.65 µH and 44.42 µH and the corresponding inductor power loss are 5.6 Watt and 8.77 Watt respectively. Therefore the required minimum inductor value to make the converter to operate in FCCM of operation for different test cases in different modes of operation must be less than 12.65 µH. Hence 10 µH is considered in circuit topology module. This 10 µH inductor is considered as optimal unique inductor value which ensures FCCM of operation in all the three modes of operation in different test cases. This inductor conduction loss lies in the range of 5.85 Watt to 43.76 Watt for different test cases in FCCM of operation.

IV. SNUBBER CAPACITOR SELECTION

To minimize the turn-off loss in larger extent, larger snubber capacitor is required which minimizes drain current during turn-off period, but it may lead to more turn-on loss, because it will not discharge fully during turn-on period. The snubber capacitor is selected in such a way that it must minimize total turn-on, turn-off and snubber capacitor loss. During switch turn ON time, capacitor voltage fully discharges when the inductor stored energy is greater than the capacitor energy storage ability. This leads to minimum turn ON loss. The charge balance of CV^2 and $\frac{1}{2}LI_L^2$ is used for snubber capacitor design as given in equation (5) for minimum turn ON loss

$$C.V^2 \leq \frac{1}{2}.L.I_L^2 \quad (5)$$

The above equation is modified for snubber capacitor value as given in equation (6) to minimize switching turn on loss as well as snubber capacitor loss.

$$C \leq 0.5.L.\left(\frac{I_L}{V}\right)^2 \quad (6)$$

Where C= snubber capacitor, V= capacitor voltage, L= Inductor and I_L = inductor average current.

The power loss in snubber capacitor is given in equation (7) [12]

$$P\_C_{SNU} = \frac{1}{2}.C_s.V_{DS}^2.f_{sw} \quad (7)$$

Where C_s is the snubber capacitor, V_{DS} is the maximum voltage across the switch and f_{sw} is the switching frequency

The snubber capacitor is optimized for minimum power loss across it and for minimum switching turn on loss to improve the efficiency. For this, series of MATLAB script are executed and results are tabulated in Table 2.

TABLE II SNUBBER CAPACITOR OPTIMIZATION

Mode of operation	Case*	$V_1=V_{DS}$ (V)	C_{SNU} (nF)	E_C_{SNU} [$C_S.V_1^2$] (Joule)	E_15nf (Joule)	E_10µH [$\frac{1}{2}.L.I_L^2$] (Joule)	P_C_{SNU} (W)	P_15nf (W)
Buck	1	249.90	18.01	0.0011	9.36e-4	0.0011	56.25	46.84
	2	249.83	32.04	0.002	9.36e-4	0.002	100	46.81
	3	249.91	32.02	0.002	9.36e-4	0.002	100	46.84
	4	269.91	15.44	0.0011	0.0011	0.0011	56.25	54.64
Boost	1	102.90	67.98	7.2e-4	1.58e-4	7.2e-4	36	7.94
	2	112.91	56.47	7.2e-4	1.91e-4	7.2e-4	36	9.56
	3	130.02	75.70	0.0013	2.53e-4	0.0013	64	12.68
	4	79.84	112.94	7.20e-4	9.56e-5	7.2e-4	36	4.78
Buck-Boost	1	249.79	72.11	0.0045	9.35e-4	0.0045	225	46.79
		250.05	31.98	0.0020	9.37e-4	0.0020	100	46.89
	2	249.82	72.09	0.0045	9.36e-4	0.0045	225	46.81
		250.07	31.98	0.0020	9.38e-4	0.0020	100	46.90
	3	259.80	66.67	0.0045	0.0010	0.0045	225	50.62
		260.05	29.57	0.0020	0.0010	0.0020	100	50.72

* Test cases as in Table 1, for different values of V_H, V_L, R_1, R_2, and I

From equation (7) the power loss in snubber capacitor is directly proportional to snubber capacitor value, drain to source voltage of MOSFET and switching frequency, so it is better to select minimum value of snubber capacitor for maximum efficiency.

From the Table 2, it is observed that, the minimum snubber capacitor value for maximum capacitor voltage is 15.44 nF and the corresponding power loss through it is 56.25 Watts. To satisfy equation (5), for all different test cases in different modes of operation, a snubber capacitor of 15nF is considered in circuit topology module, which is considered as optimal unique snubber capacitor value for all the three modes of operation. This ensures, the capacitor fully discharge before the switch is turn on, which minimizes the switch turn-on loss.

V. CONCLUSION

The paper presents a high-efficiency bidirectional non-isolated synchronous DC-DC switching power converter. The converter is made to operate in Forced Continuous Current Mode (FCCM)/ Synchronous Discontinuous Current Mode (SDCM) of operation, to minimize the inductor value, size, cost and weight of the converter. The turn off loss of the switch induced by SDCM of operation is minimized by connecting snubber capacitor across the transistor switch. A complementary gate signal control scheme is used to turn on and off the transistor switch. Anti-paralleled diode of the transistor switch helps to discharge the capacitor. SDCM of operation due to complementary control gate signal scheme, minimum turn on loss of the transistor switch and low diode reverse recovery loss are achieved. Thus the Zero Voltage Resonant Transition (ZVRT) of transistor switch is realized, both turn on and turn off loss is minimized and also removes the parasitic ringing in inductor current. A serial of MATLAB script are executed to find the optimum value of snubber capacitor and inductor based on the minimal overall device and switch conduction loss condition.

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