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Analysis of Threshold Voltage of Biaxial Strained Silicon nMOSFET

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***Abstract* - For nanoscale CMOS applications, strained-silicon devices have been receiving considerable attention owing to their potential for achieving higher performance and compatibility with conventional silicon processing. In this work we present the analysis of effect of strain on threshold voltage of biaxial strained-Si/Si_{1-x} Ge_x nMOSFET taking into consideration the quantum mechanical effect (QME).**

Keywords : **Biaxial Strained Silicon MOSFET, QME, Threshold Voltage, Si_{1-x} Ge_x**

I. Introduction

Silicon–based MOSFETs have reached remarkable levels of performance through device scaling. However, it is becoming increasingly hard to improve device performance through traditional scaling method. Strained-silicon devices have been receiving considerable attention owing to their potential for achieving higher performance due to improved carrier-transport properties, i.e. mobility and high-field velocity [1]. Literature survey shows an improvement in static and dynamic CMOS circuit performance has been demonstrated using as strained-Si/Si_{1-x} Ge_x MOSFETs.

As the transistor gate length drops to 32 nm and below and the gate effective oxide thickness drops to 1 nm [1, 2], physical limitations, such as reduction in drive currents, make geometric scaling an increasingly challenging task. One of the approaches is to increase the carrier mobility in the active region of the device by introducing strain. Starting with the 90-nm technology generation, mobility enhancement through uniaxial process-induced-strained Si has emerged as the next scaling vector being widely adopted in logic technologies [3]. Presently with the 65nm logic technology in volume production and 45 nm and 32 nm under development, all featuring strained Si state-of the art technology. The strained silicon technologies have been analysed and very few commercially viable devices have been produced.

The aim of this paper is to present analysis of threshold voltage taking into consideration the QME and strain. The threshold voltage of the strained Si/Si_{1-x} Ge_x is calculated for different germanium mole fractions, doping concentration, oxide thickness as well as thickness of strained silicon layer.

II. QUANTUM MECHANICAL MODEL

The aggressive downscaling methodgy of device dimensions in CMOS technology relies that the use of successively thinner gate dielectrics and higher levels of channels doping as feature sizes decrease in order to simultaneously achieve the desired device turn–off and drive current capabilities [2]. As gate lengths approaches deep submicron dimensions ≤10 nm, the device design as guided by scaling , can result in very large transverse electric field at the Si/SiO_2 interface, even near the threshold of inversion. This leads to significant bending of the energy bands at the Si/SiO_2 interface [2]. In this case, the potential well can become narrow to quantize the motion of inversion layers carriers in the direction perpendicular to the interface. This gives rise to a splitting of the energy levels into subbands (two dimensional (2-D) density of states), such that the lowest of the allowed energy levels for electrons in the well does not coincide with the bottom of the conduction band. As the surface electric field increases, the system becomes more and more quantized more and more carriers become confined in the potential well. Because of the smaller density of states in the 2-D system, the total population of the carriers will be smaller for the same Fermi-level than in the corresponding 3-D (or classical) case. This phenomena will affect the net sheet charge of carriers in the inversion layers, thus requiring a large gate voltage in order to populate a 2-D inversion layer to have the same number of carriers as the corresponding 3-D system. This will have an impact on the threshold voltage of a MOSFET, an important parameters in the deep submicron design, especially as the power supply voltage drop to lower levels [3, 4]

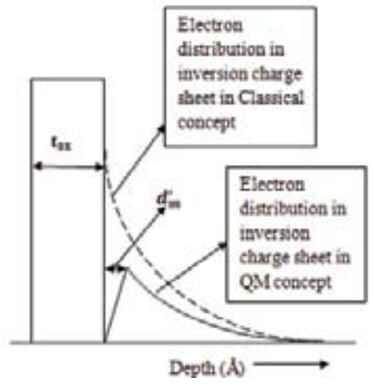

Fig.1Comparison of the predicted electron charge distribution in inversion layer for both classical and QM models.

In classical treatments of the inversion layer, the charge distribute is the peaked at the Si/SiO_2 interface because that is where the band bending and electric is the greatest. However, in a quantized(2-D) system, the carrier concentration is very low at the interface, and the peak is displayed away from the interface (due to the wave nature of the inversion layers carriers). This comparison between the simulated spatial distribution of electron in the inversion layer for both the classical and quantum mechanical (QM) predictions is shown in figure 1. The displacement of charge further away from the gate electrode cases a decrease in the oxide capacitance (looks an increase in the electrical oxide thickness) [4,5,6]. In older generations of technology , where the physical oxide thickness was thicker than oxides used in deep submicron technologies, this increase in the effective oxide thickness was a very small fraction of the total gate capacitance, so that the effect was not significant at the room temperature. However, in technologies with deep submicron design rules, the increase in the electrical oxide thickness due to the displacement of the charge away from the interface can be a significant fraction of the physical oxide thickness. It is important to account for QMEs in the inversion layer in deep submicron device design. The use of the traditional, or classical, models in device analysis and design in which these effects are neglected, is inadequate at deep submicron dimensions and will lead to erroneous and misleading predications of the device structure and electrical behavior, such as the physical oxide thickness, linear reason threshold voltage, drive current, capacitance, on-state series resistance.

III. The Cross-Section of Nanoscale Bulk Strained - Si/$Si_{1-X}Ge_x$ n Mosfet

The cross-section of the nanoscale bulk strained- Si/$Si_{1-x}Ge_x$ MOSFET considered in this study is shown in figure 2.The low field mobility of the carriers (μ_{eff}) is enhanced due to strain in Si thin films grown pseudomorphically over a relaxed $Si_{1-x}Ge_x$ substrate. However, for short channels devices, high – field effects like velocity saturation work against this enhancement. The velocity overshoot become prominent as MOSFET dimensions shrinks to the nanoscale regime, and this is directly related with the improvement in the drive current observed in short –channel MOSFETs. It has been seen that an electric field step can result in the electron velocity when exceeds the saturation velocity for a period shorter than the energy relaxation time t_w (which is an average time constant associated with the energy scattering process, or the time needed by the electron to once again reach equilibrium with the energy scattering process, or the time needed by electron to once again reach equilibrium with the lattice), thus causing the electron to approach ballistics transport conditions. Strain in the silicon thin film also leads to an increase in the energy relaxation time of the carriers, thus increasing the velocity overshoot. Hence current enhancement in short channel strained –Si devices [1].

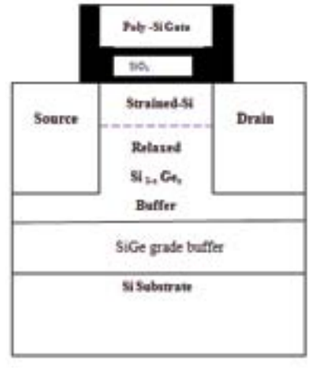

Fig. 2 Cross-sectional view of the strained $Si/Si_{1x}Ge_x$ MOSFET

IV. The Modified Threshold Voltage Model

We have used the classical definition of threshold voltage that refers to the gate voltage for which the inversion Layer electron concentration at the interface become equal to the bulk hole concentration for n-MOSFETs. Thus the threshold voltage V_{th} of a MOSFET can be determine by knowing the three potential functions: (1) the voltage drop across the semiconductor (ϕ_s) when the surface electron concentration equals the quasi-neutral hole concentration, (2) the oxide potential drop (ϕ_{ox}) under same condition and (3) the flat band voltage V_{FB}, the gate voltage for which the total integrated charge in the semiconductor becomes zero. The subscript sS stand for strained-Si and x refers to the germanium mole fraction in $Si_{1-x}Ge_x$ and band gap of material. Surface potential is one of important part which plays an important role in calculation for threshold voltage for a strained-Si/$Si_{1-x}Ge_x$ nMOSFET, which is calculated by following relation is given by (1) has calculated as

$$\Phi_s^{Ss} = 2\Phi_B^{sS} = \frac{qN_a W_{dm}^{n[sS]}}{2\epsilon_{si}} \quad (1)$$

The classical threshold condition corresponding to the onset of strong inversion at $\phi_{sS}=2\phi_B^{sS}$, for strained silicon W_{dm}^{sS} is the modified depletion depth [17]. For biaxial-strained and ϕ_B^{sS} is bulk potential is calculated by

$$\Phi_B^{sS} = \frac{kT}{q} log\left(\frac{N_a}{n_i^{sS}}\right) \quad (2)$$

where n_i^{sS} [cm^{-3}] is the intrinsic carrier concentration for strained silicon and N_a is the doping concentration in [cm^{-3}], q is the electronics charge, k is the Boltzmann constant and T is the temperature respectively. Intrinsic carrier concentration, which is give by

$$n_{i,sS} = \sqrt{N_c N_v} exp\left(-\frac{E_{g,sS}}{2kT}\right) \quad (3)$$

Ensergy band gap of biaxial strained silicon layer is given by, $E_{g,sS}$=1.084-x(0.31+0.53x) [5]. N_c and N_v denote the density of states functions at the conduction band and valance band edges, respectively,. The subscript sS stand for strained Si; x and $E_{g,sS}$ respectively , refer to the germanium mole fraction in $Si_{1-x}Ge_x$ and band gap of material. When the quantum–mechanical approximation has been made, surface potential is changed [5, 7]. Now modified surface potential for is given by

$$\Phi_{s,md}^{sS} = \Phi_s^{sS} + \Delta\Phi_{S[sS]}^{QM} \quad (4)$$

Increased surface potential after taking QM effect can be estimated by following (4) and (5)

$$\Delta\Phi_{s,QM} = \frac{qN_a}{2\epsilon_{Si}}\left(d_{cl} + \frac{9}{4\alpha_T}\right)^2 - 2\Phi_B \quad (5)$$

Oxide potential is the second important factor which also plays a significant role in threshold calculation. The oxide potential can be calculated by following relations

$$\Phi_{ox}^{sS} = \gamma\left(\sqrt{\Phi_s^{sS}}\right) \quad (6)$$

where r the body coefficient is defined as $\gamma = \sqrt{(2\epsilon_{si}qN_a)}/C_{ox}$, C_{ox} being the oxide capacitance per unit area in the inversion, and ϵ_{Si} is the average permittivity of the strained–Si and $Si_{1-x}Ge_x$ layers. As mentioned in section 2, the physical oxide thickness is slightly increased, when considering QM effect, named effective oxide thickness and modified expression for effective oxide thickness is written as [5, 12]

$$t_{ox}^{md} = t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{Si}} d_m' \quad (7)$$

where d'$_m$ is changed in depletion depth due QME is shown in fig. and defined by (6). As result, the modified oxide potential will be give by

$$\Phi_{s,md}^{sS} = \Phi_s^{sS} + \Delta\Phi_{S[sS]}^{QM} \quad (8)$$

where is the body effect coefficient which also changed the modified expression is shown by Eq.8

$$\gamma_{md} = \frac{\sqrt{2qN_a\varepsilon_s}}{C_{ox}^{md}} \quad (9)$$

In (9) C_{ox} being the oxide capacitance per unit area in inversion, and e_s is the average permittivity of the strained-silicon and $Si_{1-x}Ge_x$ layer. Due to QM effect the expression for $C_{ox\ is}$ also changed, the modified expression for C_{ox} is expressed by (10)

$$C_{ox}^{md} = \frac{\varepsilon_{ox}}{t_{ox}^{md}} \quad (10)$$

In (6) d'$_m$ is expressed by following expression as given by

$$d_m' = \frac{9}{4\alpha_{T[sS]}} \quad (11)$$

Here $б_{T[sS]}$ in case of biaxial strained MOSFET is defined as

$$\alpha_{T[sS]} = \left[\frac{3m_d^{*2}N_a d_{cl}^{sS}}{2\varepsilon_{Si}\hbar^2}\right] \quad (12)$$

Quantum mechanical effect also changes flat band potential, the modified potential is presented by

$$V_{FB}^{md} = V_{FB} + qN_a\left(\frac{d_m'}{2\varepsilon_{Si}} + \frac{t_{ox}^{md}}{\epsilon_{ox}}\right) \quad (13)$$

In (15) all used variables have usual meaning and defined by (6) and (10) and ϵ_{ox} and ϵ_{Si} are respectively, the permittivity of SiO_2 and silicon. Considering the above-noted three effects as described in (4), (7) and 13; the threshold voltage for strained-Si channel MOSFET can be expressed as

$$V_{th}^{sS} = V_{FB}^{corrected} + \phi_{s,md}^{sS} + \phi_{ox}^{md} \quad (14)$$

V. Results And Discussion

The values of the various material and transport parameters to strained Si grown on the $Si_{1-x}Ge_x$ layer has been reported in the literature for wide range of x from up to a value exceeding 0.5[5]. In our calculation threshold voltage of strained –Si MOSFETs for x values in the rang 0.4 as strain in Si is more likely to get relaxed. In our calculations we have used the QM concept for developing analytical equation of V_{th} for strained-Si MOSFETs. The additional oxide thickness d'$_m$, which account for quantum-mechanical effects on the distribution of the inversion charge.

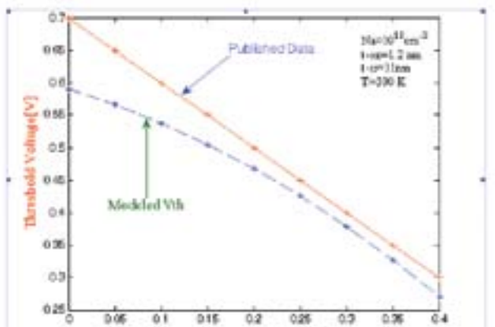

Fig. 3 Variation of threshold voltage for various Ge mole fraction and bench marking with publish data

Figure 3 displays the variation of threshold voltage against Ge mole fraction x and bench marking with published data. One can observe that our analytical results are in closer agreement with published data.

A comparison of results from proposed model with the unstrained without QM effect and with QM effect against Ge mole fraction x is done in figure 4. It is observed that at the same doping concentration threshold voltage is less in strained-Si MOSFET. This result is good agreement with literature survey and published data. One can also observe strained- Si technique minimizes QM at higher doping concentration.

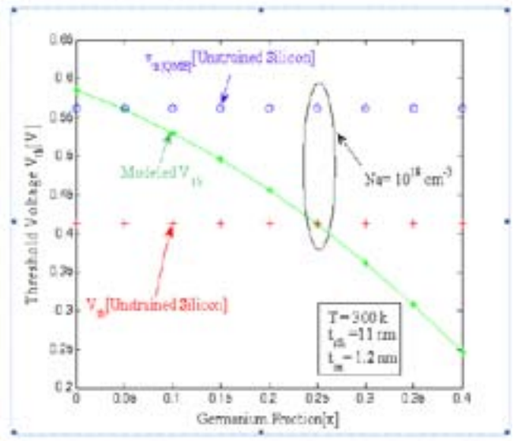

Fig. 4 Variation of threshold voltage against germanium mole fraction and comparison with unstrained silicon MOSFETs.

Figure 4 shows that the threshold voltage decreases for a higher value of x and the same doping concentration in strained-Si MOSFET threshold voltage lesser than unstrained silicon MOSFET. As x increases, the conduction and valance band offset also rise [3,5], thereby decreasing the value surface potential ($\phi^{sS}S$), the drop in ϕsSS causes a decrease in threshold voltage.

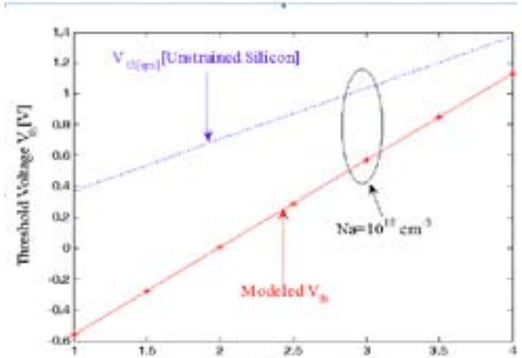

Fig. 5Variation of threshold voltage against oxide thickness and comparison with unstrained silicon MOSFETs.

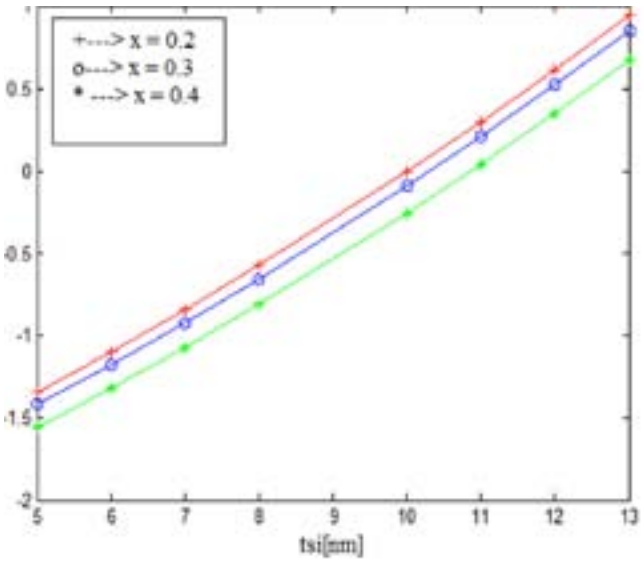

Fig. 6 Variation of threshold voltage against Starined silicon thickness t_{si}

A comparison of modified model results and unstrained Si MOSFETs including QM effect against oxide thickness (to_x) are shown in figure 5. It is observed that at the same doping concentration threshold voltage is less in strained-Si MOSFET. Also the variation of threshold voltage against strained silicon thickness tsi can be observed in figure 6. In modern CMOS technology for better MOSFET performance a small oxide thickness is desired, which also causes QM effect , resulting increase in surface potential as well as threshold voltage (V^{th}).For the same doping concentration threshold voltage is lesser in strained-Si MOSFET.

VI. Conclusion

A physics based simple analytical model for the threshold voltage of strained-Si-Si_{1-x} Ge_x MOSFET is presented and the effect of various design parameters has been analysed. The threshold voltage is sensitivity to electron affinity, bandgap of the strained- Si epitaxial layer, substrate doping and the thickness of strained silicon layer has been analysed. Modeled results show that the threshold voltage of nanoscale MOSFET can be altered by careful selection of the device design parameters. It is clear that in strained-Si MOSFET QM effect on threshold voltage can therefore be minimized and can be controlled.

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